19-0593; Rev 1; 1/07

EVALUATION KIT AVAILABLE

2.5MHz/1.5MHz Step-Down Converters with 60mΩ Bypass in TDFN for CDMA PA Power

MAX8581/MAX8582

General Description

The MAX8581/MAX8582 high-frequency step-down converters are optimized for dynamically powering the power amplifier (PA) in CDMA handsets. They integrate a high-efficiency PWM step-down converter for medium- and low-power transmission and a 60mΩ (typ) bypass mode to power the PA directly from the battery during high-power transmission. They use an analog input driven by an external DAC to control the output voltage linearly for continuous PA power adjustment. The MAX8581/MAX8582 use an internal feedback network, and the switching frequency is internally set to 2.5MHz and 1.5MHz, respectively.

Fast switching (up to 2.5MHz) and fast soft-start allow the use of ceramic 2.2µF input and output capacitors while maintaining low voltage ripple. The small 1.5µH to 3.3µH inductor size can be optimized for efficiency.

The MAX8581/MAX8582 are available in 10-pin, 3mm x 3mm TDFN packages (0.8mm max height).

Features

- ♦ **600mA Step-Down Converter**
- ♦ **60mΩ (typ) Bypass Mode with Integrated FET**
- ♦ **Dynamically Adjustable Output from 0.4V to V_{IN}**
- ♦ **2.5MHz and 1.5MHz Switching Frequency**
- ♦ **Small LC Components: 1.5µH to 3.3µH and 2.2µF**
- ♦ **Up to 94% Efficiency**
- ♦ **Low Output Ripple at All Loads**
- ♦ **2.7V to 5.5V Input**
- ♦ **0.1µA Shutdown Mode**
- ♦ **Output Short-Circuit Protection**
- ♦ **Thermal Shutdown**
- ♦ **10-Pin, 3mm x 3mm TDFN Packages**

Applications

WCDMA/NCDMA Cell Phones

Wireless PDAs, Smartphones

Ordering Information

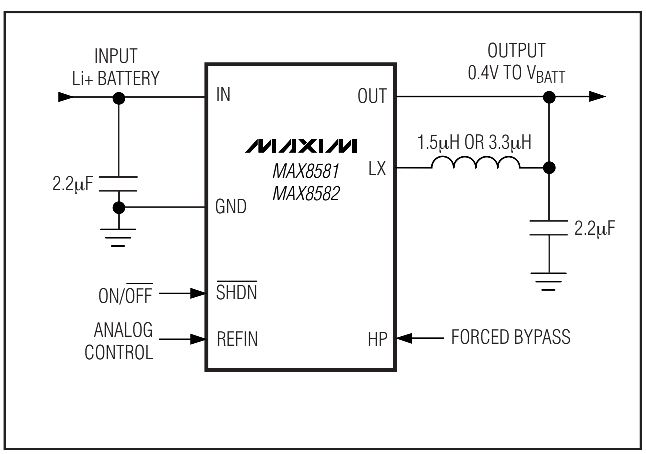
PART*	PIN-PACKAGE	TOP MARK	PKG CODE
MAX8581ETB+	10 TDFN-EP**	ACT	T1033-1
MAX8582ETB+	10 TDFN-EP**	ACU	T1033-1

*All devices are specified in the -40°C to +85°C extended temperature range.

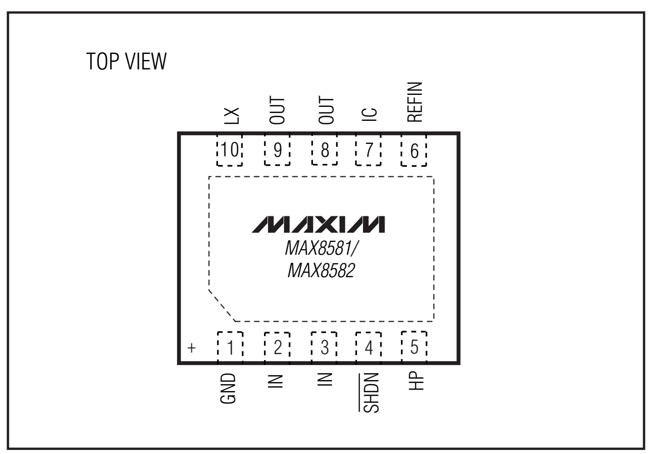
**EP = Exposed pad.

+Denotes a lead-free package.

Typical Operating Circuit



Pin Configuration



ABSOLUTE MAXIMUM RATINGS

IN, $\overline{SHDN}$, HP, REFIN to GND ....-0.3V to +6.0V
LX, OUT, IC to GND....................................-0.3V to (V_{IN} + 0.3V)
OUT Short Circuit to GND ....Continuous
LX Current ....$0.7A_{RMS}$
IN, OUT Current..$2.5A_{RMS}$

Continuous Power Dissipation (T_A = +70°C)
10-Pin TDFN (derate 24.4mW/°C above +70°C).........1951mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = $V_{\overline{SHDN}}$ = 3.6V, V_{REFIN} = 0.9V, V_{HP} = V_{IC} = 0V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
Supply Voltage Range	V_{IN}		2.7		5.5	V
UVLO Threshold	UVLO	V_{IN} rising, 180mV hysteresis	2.55	2.63	2.70	V
Supply Current	I_{IN}	I_{LOAD} = 0A, switching at 1.5MHz		4000		µA
Supply Current	I_{IN}	Shutdown, T_A = +25°C		0.1	10	µA
Supply Current	I_{IN}	Shutdown, T_A = +85°C		1.0		µA
OUT						
OUT Voltage Accuracy	V_{OUT}	V_{IN} = 4.2V, V_{REFIN} = 1.7V	3.33	3.40	3.47	V
OUT Voltage Accuracy	V_{OUT}	V_{IN} = 3.6V, V_{REFIN} = 0.9V	1.75	1.80	1.85	V
OUT Voltage Accuracy	V_{OUT}	V_{IN} = 3.6V, V_{REFIN} = 0.4V	0.75	0.80	0.85	V
OUT Input Resistance	R_{OUT}	V_{LX} = V_{OUT}, MAX8581		360		kΩ
OUT Input Resistance	R_{OUT}	V_{LX} = V_{OUT}, MAX8582		558		kΩ
REFIN						
REFIN Common-Mode Range			0		2.2	V
REFIN to OUT Gain				2.00		V/V
REFIN Input Resistance				518		kΩ
REFIN Dual Mode™ Threshold		V_{REFIN} rising, 77mV hysteresis	0.45 x V_{IN}	0.463 x V_{IN}	0.475 x V_{IN}	V
LOGIC INPUTS						
Logic Input Level	V_{IH}	V_{IN} = 2.7V to 5.5V	1.4			V
Logic Input Level	V_{IL}	V_{IN} = 2.7V to 5.5V			0.4	V
Logic Input Bias Current	I_{IH}, I_{IL}	V_{INPUT} = 0V or V_{IN}, T_A = +25°C		0.01	1	µA
Logic Input Bias Current	I_{IH}, I_{IL}	V_{INPUT} = 0V or V_{IN}, T_A = +85°C		0.1		µA

Dual Mode is a trademark of Maxim Integrated Products, Inc.

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = V_{\overline{SHDN}}$ = 3.6V, V_{REFIN} = 0.9, $V_{HP} = V_{IC}$ = 0V, T_A = -40°C to +85°C, typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LX							
On-Resistance	R_{ONP}	p-channel MOSFET switch, I_{LX} = -40mA			0.2	0.4	Ω
	R_{ONN}	n-channel MOSFET rectifier, I_{LX} = 40mA			0.18	0.35	
LX Leakage Current	I_{LXLKG}	V_{IN} = 5.5V, LX = GND	T_A = +25°C		0.1	5	µA
			T_A = +85°C		1		
p-Channel MOSFET Peak Current Limit	I_{LIMP}			700	1077	1400	mA
n-Channel MOSFET Valley Current Limit	I_{LIMN}			790	985	1150	mA
Minimum On- and Off-Times	$t_{ON(MIN)}$			70	114	150	ns
	$t_{OFF(MIN)}$			70	112	150	
t_{ON}/t_{OFF} Ratio		$t_{ON(MIN)} / t_{OFF(MIN)}$		0.90	1.02	1.13	s/s
Switching Frequency		MAX8581			2.5		MHz
		MAX8582			1.5		
BYPASS							
On-Resistance	R_{ONBYP}	p-channel MOSFET bypass, I_{OUT} = -400mA, T_A = +25°C			0.06	0.1	Ω
		p-channel MOSFET bypass, I_{OUT} = -400mA				0.12	
Bypass Current Limit				1.0	2.1		A
Step-Down Current Limit in Bypass				700	1077	1400	mA
GENERAL							
Thermal Shutdown					+160		°C
Thermal-Shutdown Hysteresis					20		°C
Power-Up Delay		$V_{\overline{SHDN}}$ rising to V_{LX} rising			50	130	µs

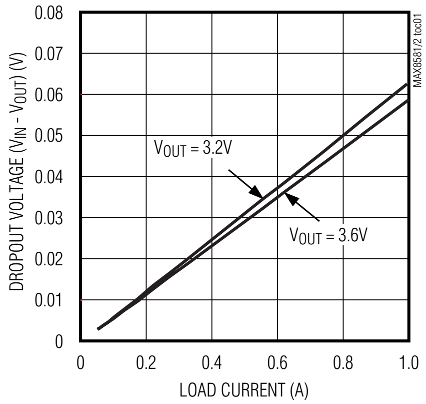
Note 1: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

2.5MHz/1.5MHz Step-Down Converters with 60mΩ Bypass in TDFN for CDMA PA Power

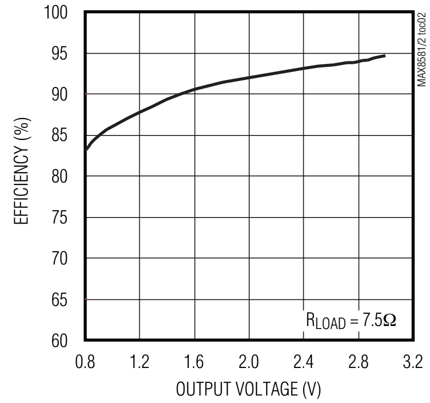
Typical Operating Characteristics

(V_{IN} = 3.6V, V_{OUT} = 1.2V, MAX8582 EV Kit, T_A = +25°C, unless otherwise noted.)

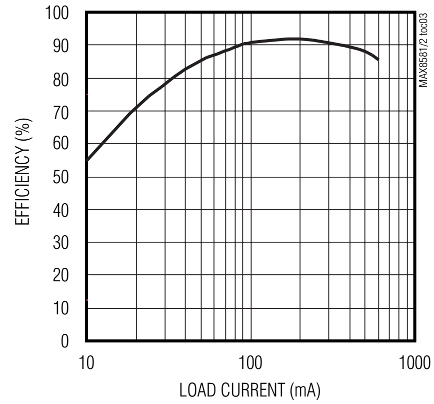
BYPASS MODE DROPOUT VOLTAGE vs. LOAD CURRENT



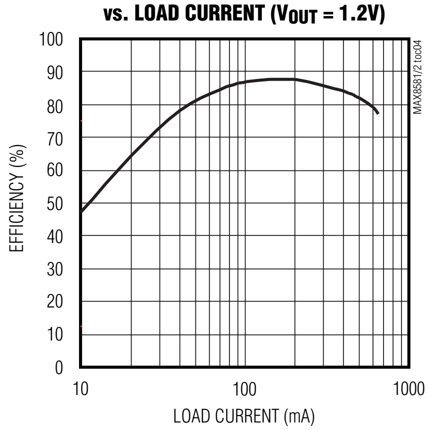
EFFICIENCY vs. OUTPUT VOLTAGE



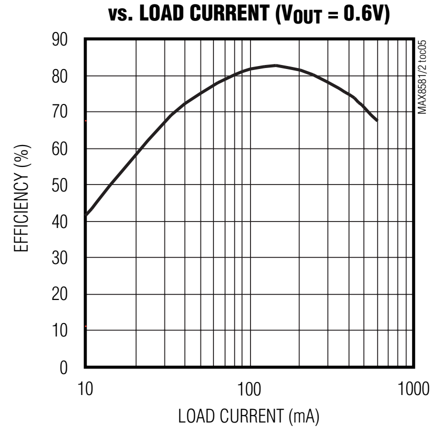
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.8V)



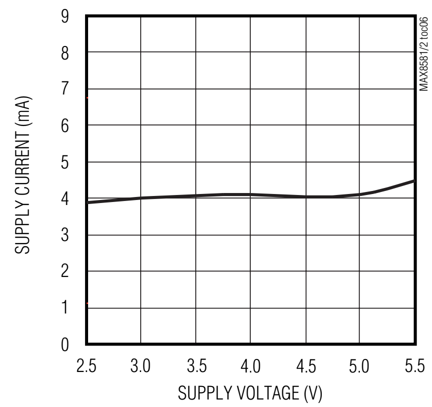
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.2V)



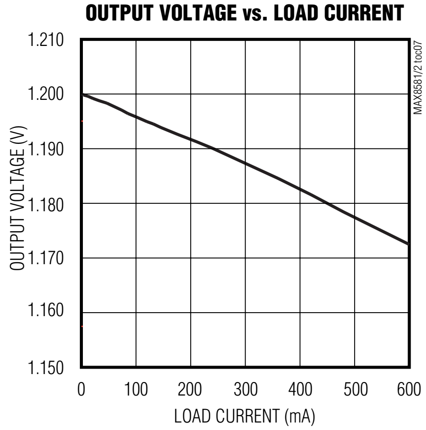
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 0.6V)



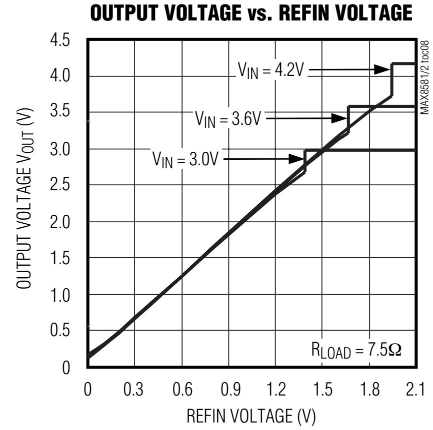
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



OUTPUT VOLTAGE vs. LOAD CURRENT



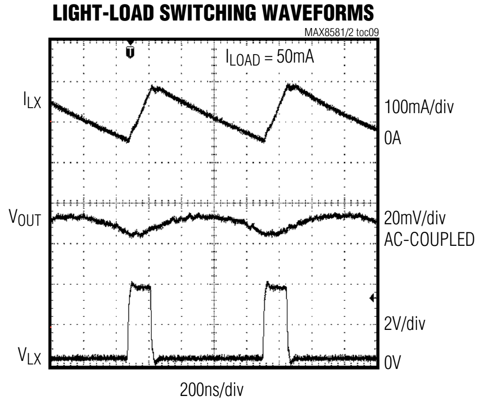
OUTPUT VOLTAGE vs. REFIN VOLTAGE



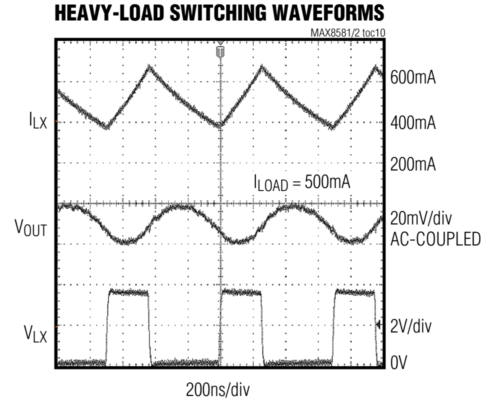
Typical Operating Characteristics (continued)

(V_{IN} = 3.6V, V_{OUT} = 1.2V, MAX8582 EV Kit, T_A = +25°C, unless otherwise noted.)

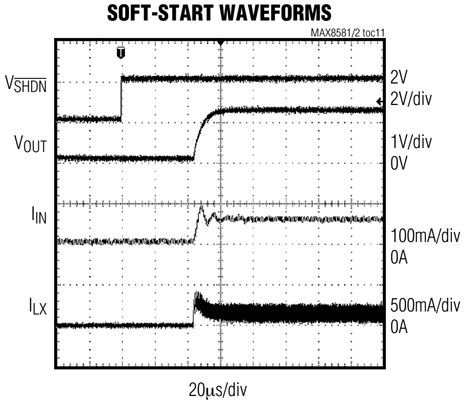
LIGHT-LOAD SWITCHING WAVEFORMS



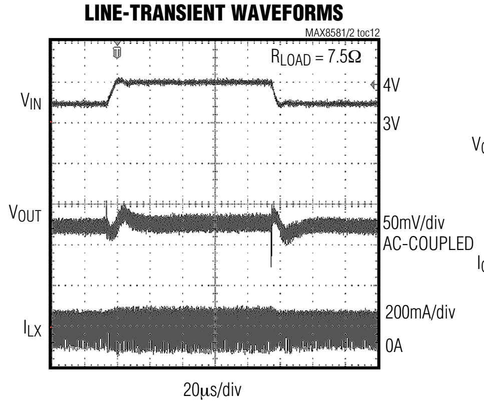
HEAVY-LOAD SWITCHING WAVEFORMS



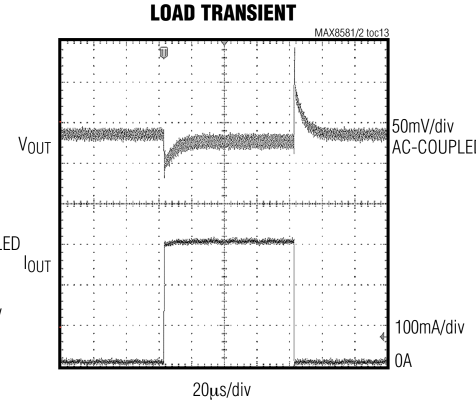
SOFT-START WAVEFORMS



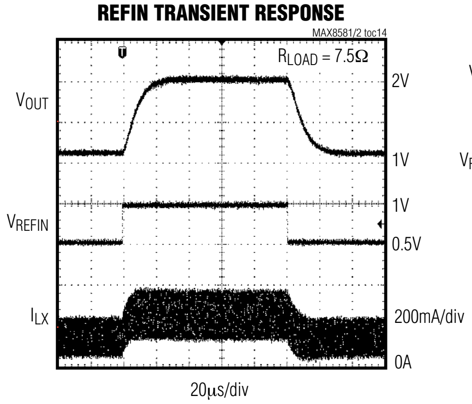
LINE-TRANSIENT WAVEFORMS



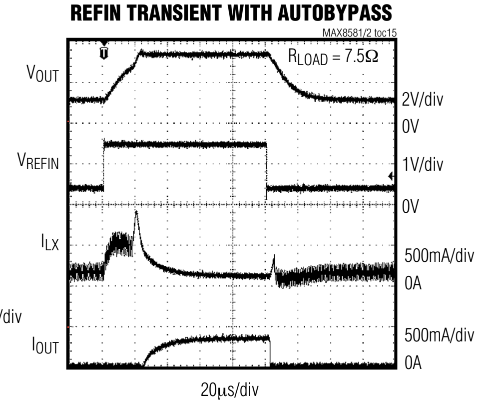
LOAD TRANSIENT



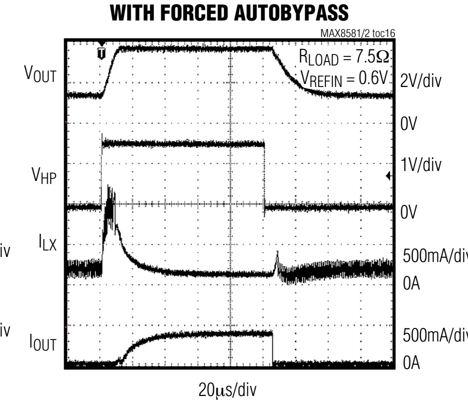
REFIN TRANSIENT RESPONSE



REFIN TRANSIENT WITH AUTOBYPASS



HP TRANSIENT RESPONSE WITH FORCED AUTOBYPASS



2.5MHz/1.5MHz Step-Down Converters with 60mΩ Bypass in TDFN for CDMA PA Power

Pin Description

PIN	NAME	FUNCTION
1	GND	Ground
2, 3	IN	Supply Voltage Input. 2.7V to 5.5V. Bypass with a 2.2µF ceramic capacitor as close as possible to IN and GND.
4	$\overline{SHDN}$	Active-Low Shutdown Input. Connect to IN or logic-high for normal operation. Connect to GND or logic-low for shutdown mode.
5	HP	High-Power Mode Set Input. Drive HP high to invoke bypass mode. Bypass mode connects IN directly to OUT with the internal bypass MOSFET.
6	REFIN	DAC-Controlled Input. Output regulates to 2 x V_{REFIN} for the MAX8581 and MAX8582. Dual-mode threshold at 0.465 V_{IN} enables bypass mode.
7	IC	Internally Connected. Connect to ground.
8, 9	OUT	Output Voltage Connection for Bypass Mode. Internally connected to IN using the internal bypass MOSFET during bypass mode. Connects to the internal feedback network.
10	LX	Inductor Connection. Connect inductor to the drains of the internal p-channel and n-channel MOSFETs. Connects to the internal feedback network.
—	EP	Exposed Paddle. Connect to GND.

Detailed Description

The MAX8581/MAX8582 step-down converters deliver over 600mA to dynamically power the PA in CDMA handsets. The hysteretic PWM control scheme switches with nearly fixed frequency at 1.5MHz (MAX8582) to 2.5MHz (MAX8581), allowing efficiency and tiny external components. A 60mΩ bypass mode connects the PA directly to the battery during high-power transmission.

Control Scheme

A hysteretic PWM control scheme ensures high efficiency, fast switching, fast transient response, low output ripple, and physically tiny external components. This control scheme is simple: When the output voltage is below the regulation voltage, the error comparator begins a switching cycle by turning on the high-side switch. This switch remains on until the minimum on-time expires and the output voltage is in regulation or the current-limit threshold is exceeded. Once off, the high-side switch remains off until the minimum off-time expires and the output voltage falls out of regulation. During this period, the low-side synchronous rectifier turns on and remains on until the high-side switch turns on again. The internal synchronous rectifier eliminates the need for an external Schottky diode.

Voltage-Positioning Load Regulation

The MAX8581/MAX8582 utilize a unique feedback network. By taking feedback from the LX node, the usual phase lag due to the output capacitor is removed, making the loop exceedingly stable and allowing the use of very small ceramic output capacitors. This configuration yields load regulation equal to half the inductor's series resistance multiplied by the load current. This voltage-positioning load regulation greatly reduces overshoot during load transients or when changing V_{OUT} from one voltage to another. However, when calculating REFIN voltage, the load regulation should be considered. Because inductor resistance is typically well specified and the typical PA is a resistive load, the V_{REFIN} to V_{OUT} gain is slightly less than 2V/V for the MAX8581/MAX8582.

Bypass Mode

During high-power transmission, the bypass mode's low on-resistance provides low dropout, long battery life, and high output-current capability. Bypass mode connects IN directly to OUT with the internal 60mΩ (typ) bypass FET, while the step-down converter is forced into 100% duty-cycle operation to slightly lower total on-resistance to less than 60mΩ (typ).

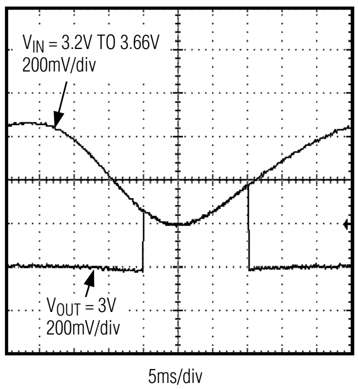


Figure 1. V_{IN} and V_{OUT} with Automatic Entry/Exit into Bypass Mode

Forced and Automatic Bypass Mode

Invoke forced-bypass mode by driving HP high or invoke automatic bypass by applying a high voltage to REFIN (V_{REFIN} > 2.1V with a Li-ion (Li+) battery at IN).

To prevent excessive output ripple as the step-down converter approaches dropout, the MAX8581/MAX8582 preemptively enter bypass mode automatically when $V_{REFIN} > 0.465\ V_{IN}$ (see Figure 1).

Shutdown Mode

Connect $\overline{SHDN}$ to GND or logic-low to place the MAX8581/MAX8582 in shutdown mode and reduce supply current to 0.1µA. In shutdown, the control circuitry, internal switching MOSFET, and synchronous rectifier turn off and LX becomes high impedance. Connect $\overline{SHDN}$ to IN or logic-high for normal operation.

Fast Soft-Start

The MAX8581/MAX8582 have internal fast soft-start circuitry that limits inrush current at startup, reducing transients on the input source. Soft-start is particularly useful for supplies with high output impedance such as Li+ and alkaline cells. See the Soft-Start Waveforms in the *Typical Operating Characteristics.*

Analog REFIN Control

The MAX8581/MAX8582 use REFIN to set the output voltage and to switch to bypass mode. The output voltage is two times the voltage applied at REFIN minus half the IR voltage drop caused by the inductor's DC resistance for the MAX8581/MAX8582. This allows the converter to operate in applications where dynamic voltage control is required.

Applications Information

The MAX8581/MAX8582 are optimized for use with a tiny inductor and small ceramic capacitors. The correct selection of external components ensures high efficiency, low output ripple, and fast transient response.

Setting the Output Voltage

The MAX8581/MAX8582 output voltages are set by the voltage applied to REFIN. The output voltage is 2 V_{REFIN} minus half the IR voltage drop caused by the inductor's DC resistance for the MAX8581/MAX8582.

Inductor Selection

The MAX8581/MAX8582 use 1.5µH and 3.3µH, respectively. Low inductance values are physically smaller but require faster switching, which results in some efficiency loss (see the *Typical Operating Characteristics* for efficiency).

The inductor's DC current rating only needs to match the maximum load of the application because the MAX8581/MAX8582 feature zero current overshoot during startup and load transients. For optimum transient response and high efficiency, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range.

Output Capacitor Selection

The output capacitor is required to keep the output voltage ripple small and to ensure regulation loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the unique feedback network, the output capacitance can be very low. In most applications, 2.2µF works well. For optimum load-transient performance and very low output ripple, the output capacitor value can be increased.

Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the battery or input power source and reduces switching noise in the MAX8581/MAX8582. The impedance of the input capacitor at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the MAX8581/MAX8582s' fast soft-start, the input capacitance can be very low. In most applications, 2.2µF works well. For optimum noise immunity and low input ripple, the input capacitor value can be increased.

2.5MHz/1.5MHz Step-Down Converters with 60mΩ Bypass in TDFN for CDMA PA Power

Table 1. Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (µH)	ESR (Ω)	CURRENT RATING (mA)	DIMENSIONS
Coilcraft	LP03310	1.5	0.10	1400	3.3 x 3.3 x 1.0 = 11mm³
		3.3	0.16	950	
Cooper	SD3110	1.5	0.11	970	3.1 x 3.1 x 1.05 = 10mm³
	SD3112	1.5	0.10	1090	3.1 x 3.1 x 1.2 = 12mm³
		3.3	0.17	840	
FDK	MIPF2520D	1.5	0.07	1500	2.5 x 2.0 x 1.0 = 5mm³
		3.3	0.10	1200	
Panasonic	ELC3FN	2.2	0.12	1000	3.2 x 3.2 x 1.2 = 12mm³
Sumida	CDRH2D09	1.5	0.05	680	3.2 x 3.2 x 1.2 = 12mm³
	CDRH2D11	3.3	0.10	450	
Taiyo Yuden	CB2016	2.2	0.13	510	2.0 x 1.25 x 1.45 = 3.6mm³
	CBC2016	2.2	0.20	750	
	CB2518	2.2	0.09	510	2.0 x 1.6 x 1.8 = 5.8mm³
	CBC2518	2.2	0.13	890	2.5 x 1.8 x 2.0 = 9mm³
	NR3010	1.5	0.08	1200	3.2 x 3.2 x 1.2 = 12mm³
		3.3	0.14	840	
TOKO	MDT2520-CR	2.2	0.08	700	2.5 x 2.0 x 1.0 = 5mm³
	D2812C	1.5	0.11	900	2.8 x 2.8 x 1.2 = 9.4mm³
		1.3	0.17	730	

PCB Layout Checklist

High switching frequencies and relatively large peak currents make the PCB layout a very important part of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Connect the input capacitor close to IN and GND. Connect the inductor and output capacitor as close to the IC as possible and keep their traces short, direct, and wide. Keep noisy traces, such as the LX node, as short as possible. Connect GND to the exposed paddle directly under the IC. Figure 2 illustrates an example PCB layout and routing scheme.

Chip Information

PROCESS: BiCMOS

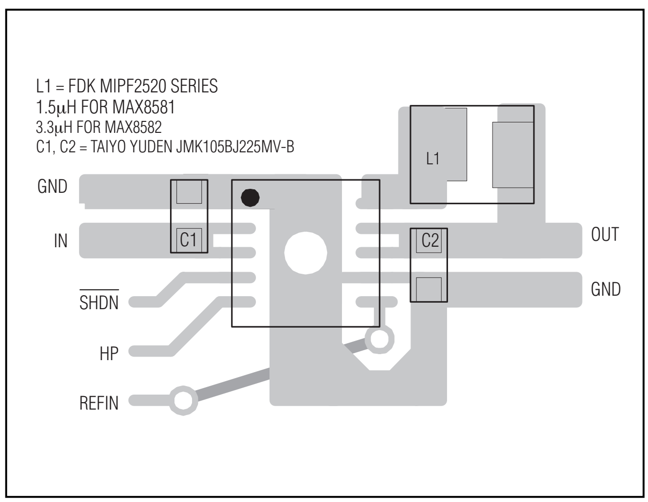
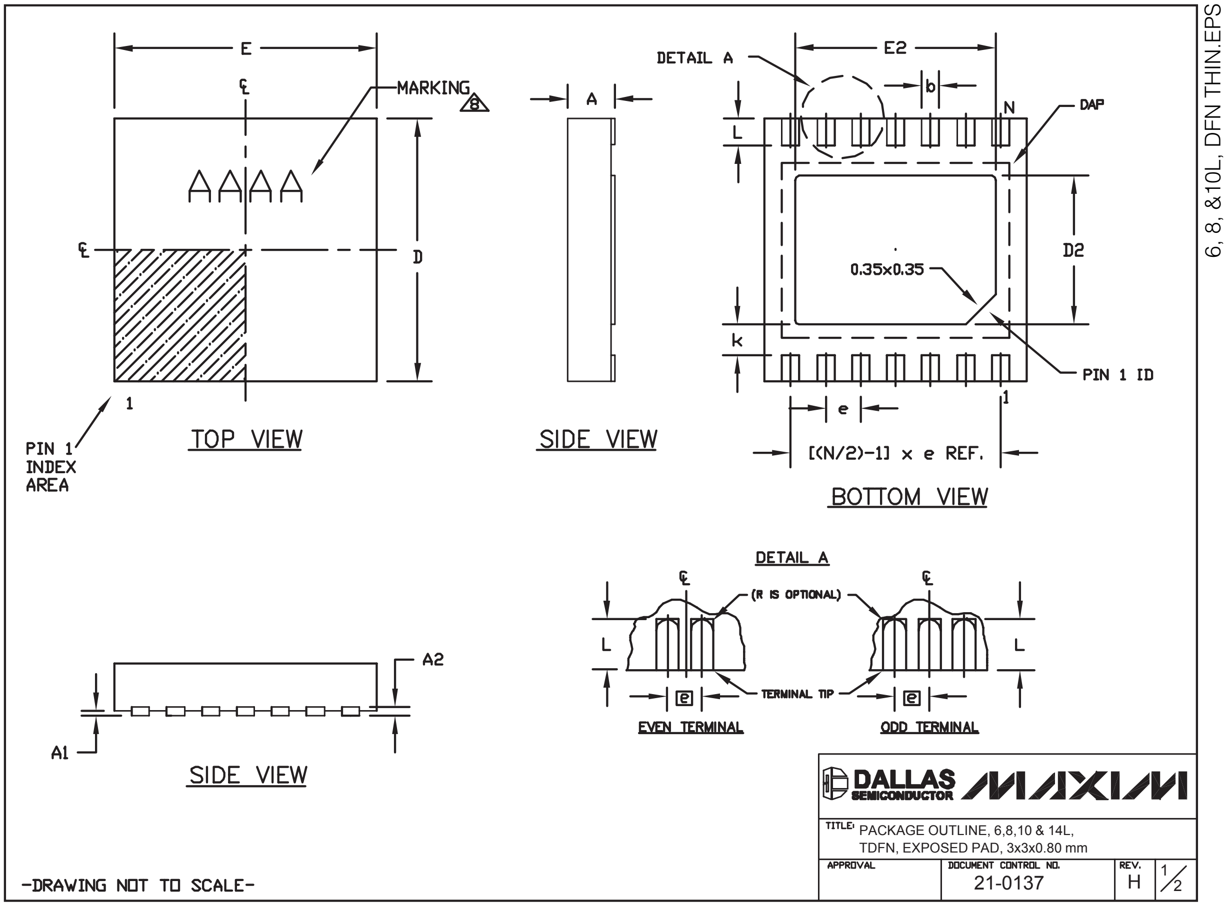


Figure 2. Example PCB Layout and Routing Scheme

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



2.5MHz/1.5MHz Step-Down Converters with 60mΩ Bypass in TDFN for CDMA PA Power

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL | DOCUMENT CONTROL NO. 21-0137 | REV. H | 2/2

-DRAWING NOT TO SCALE-

Revision History

Pages changed at Rev 1: 1, 3, 8, 9, 10